

## **QDD-800G-SR8**

### **800Gbps QSFP-DD SR8 Transceiver**

#### **1. General Description**

800Gbps Quad Small Form Factor Pluggable-Double Density (QSFP-DD) optical transceiver designed for 100 m optical communication applications.

#### **2. Features**

- Compliant to QSFP-DD/QSFP-DD800/QSFP112 HW Rev 6.2
- Compliant with CMIS 4.0
- Parallel 8 Optical Lanes
- IEEE 802.3db 800GBASE-SR8 Specification compliant
- 8x106. 25Gb/s electrical interface (800GAUI-8)
- Up to 100m transmission with OM4 MMF
- Maximum power consumption 14W
- MPO-16 Receptacle
- Single +3.3V power supply
- Case temperature range: 0 ~ +70°C
- RoHS 2.0 complaint

#### **3. Applications**

- 800G Ethernet
- Data Center Interconnect
- Enterprise Networking

#### **4. Functional Description**

This product is a 800Gb/s QSFP-DD800 SR8 optical module designed for 100m optical communication applications. The module converts 8 channels of 100Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 800Gb/s.

On the receiver side, the module converts 8 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 800Gb/s into 8 channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-16 connector can be plugged into the QSFP-DD800 SR8 module receptacle. Host FEC is required to support up to 100m fiber

transmission.

## 5. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| Parameter                 | Symbol           | Min            | Max | Units |
|---------------------------|------------------|----------------|-----|-------|
| Storage Temperature Range | T <sub>STG</sub> | -40            | 85  | °C    |
| Supply Voltage            | V <sub>CC</sub>  | 0              | 4   | V     |
| Relative Humidity         | RH               | 10% to 90%     |     |       |
|                           |                  | non-condensing |     |       |

## 6. Recommended Operating Conditions

| Parameter                   | Symbol            | Min  | Max                  | Unit |
|-----------------------------|-------------------|------|----------------------|------|
| Case Temperature- Operating | T <sub>CASE</sub> | 0    | 70                   | °C   |
| Supply Voltage              | V <sub>CC</sub>   | 3.14 | 3.46                 | V    |
| Power Consumption           | P <sub>DISS</sub> |      | 14                   | W    |
| Pre-FEC Bit Error Ratio     |                   |      | 2.4x10 <sup>-4</sup> |      |
| Link Distance over OM3      |                   | 0.5  | 60                   | M    |
| Link Distance over OM4      |                   | 0.5  | 100                  | M    |

## 7. Transmitter Optical Specifications

| Transmitter Parameter                                                                                           | Min               | Typical | Max        | Unit |
|-----------------------------------------------------------------------------------------------------------------|-------------------|---------|------------|------|
| Signaling rate each lane                                                                                        | 53.125±100ppm     |         |            | GBd  |
| Lane Wavelength Range                                                                                           |                   | 850     |            | nm   |
| RMS Spectral width                                                                                              |                   |         | 0.6        | nm   |
| Modulation Format                                                                                               | PAM4              |         |            |      |
| Average Optical Power per lane                                                                                  | -4.6              |         | 4          | dBm  |
| Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ),<br>each lane for TDECQ≤1.8dB for<br>1.8<TDECQ≤4.4dB | -2.6<br>4.4+TDECQ |         | 3.5<br>3.5 | dBm  |
| Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ),<br>each lane for TECQ≤1.8dB for 1.8<TECQ≤4.4dB      | -2.6<br>4.4+TECQ  |         | 3.5<br>3.5 | dBm  |
| Transmitter and Dispersion Eye Closure for PAM4,<br>each Lane                                                   |                   |         | 4.4        | dB   |
| Transmitter Eye Closure for PAM4(TECQ), each<br>Lane                                                            |                   |         | 4.4        | dB   |
| Extinction Ratio                                                                                                | 2.5               |         |            | dB   |
| Transmitter excursion, each lane                                                                                |                   |         | 2          | dB   |
| Transmitter transition time, each lane                                                                          |                   |         | 17         | ps   |
| Average Launch Power per Lane @ TX Off State                                                                    |                   |         | -30        | dBm  |

|                                              |                                                         |  |      |       |
|----------------------------------------------|---------------------------------------------------------|--|------|-------|
| Relative Intensity Noise <sub>12</sub> (OMA) |                                                         |  | -131 | dB/Hz |
| Optical Return Loss Tolerance                |                                                         |  | 12   | dB    |
| Encircled Flux                               | $\geq 86\%$ at 19 $\mu$ m<br>$\leq 30\%$ at 4.5 $\mu$ m |  |      | dB    |

## 8. Receiver Optical Specification

| Receiver Parameter                                                                                        | Min                 | Typical | Max              | Unit |
|-----------------------------------------------------------------------------------------------------------|---------------------|---------|------------------|------|
| Signaling rate each lane                                                                                  | 53.125 $\pm$ 100ppm |         |                  | GBd  |
| Lane Wavelength Range                                                                                     |                     | 850     |                  | nm   |
| Modulation Format                                                                                         | PAM4                |         |                  |      |
| Damage Threshold                                                                                          | 5                   |         |                  | dBm  |
| Average Receive Power, each lane                                                                          | -6.4                |         | 4                | dBm  |
| Receiver Power, each lane (OMA)                                                                           |                     |         | 3.5              | dBm  |
| Receiver Sensitivity each lane (OM <sub>Aouter</sub> ) for<br>TECQ $\leq$ 1.8dB for 1.8<TECQ $\leq$ 4.4dB |                     |         | -4.6<br>6.4+TECQ | dBm  |
| Receiver reflectance                                                                                      |                     |         | -12              | dB   |
| Stressed Receiver Sensitivity (OM <sub>Aouter</sub> ), each                                               |                     |         | -2               | dBm  |
| Stressed Conditions for Stress Receiver Sensitivity                                                       |                     |         |                  |      |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test                                                     |                     | 4.4     |                  | dB   |
| OM <sub>Aouter</sub> of each Aggressor Lane                                                               |                     | 3.5     |                  | dBm  |

## 9. Low Speed Electrical Signal

| Parameter                                    | Symbol         | Min                   | Max                   | Units | Condition                                                                |
|----------------------------------------------|----------------|-----------------------|-----------------------|-------|--------------------------------------------------------------------------|
| SCL and SDA                                  | VOL            | 0                     | 0.4                   | V     | IOL(max)=3.0mA<br>for fast mode, 20mA<br>for Fast-mode plus              |
|                                              | VOH            | V <sub>cc</sub> -0.5  | V <sub>cc</sub> +0.3  | V     |                                                                          |
| SCL and SDA                                  | VIL            | -0.3                  | V <sub>cc</sub> *0.3  | V     |                                                                          |
|                                              | VIH            | V <sub>cc</sub> *0.7  | V <sub>cc</sub> +0.5  | V     |                                                                          |
| Capacitance for SCL<br>and SDA I/O pin       | C <sub>i</sub> |                       | 14                    | pF    |                                                                          |
| Total bus capacitive load<br>for SCL and SDA | C <sub>b</sub> |                       | 100                   | pF    | 3.0k Ohms Pull up<br>resistor, max                                       |
|                                              |                |                       | 200                   | pF    | 1.6k Ohms Pull up<br>resistor, max                                       |
| LPMode/TxDis, Reset<br>and ModeSelL          | VIL            | -0.3                  | 0.8                   | V     | I <sub>lin</sub>   $\leq$ 125uA for<br>V <sub>in</sub> < V <sub>cc</sub> |
|                                              | VIH            | 2                     | V <sub>cc</sub> + 0.3 | V     |                                                                          |
| IntL/RxLOS                                   | VOL            | 0                     | 0.4                   | V     | IOL=2.0mA                                                                |
|                                              | VOH            | V <sub>CC</sub> - 0.5 | V <sub>CC</sub> + 0.3 | V     | 10k ohms pull-up<br>to Host V <sub>cc</sub>                              |

|         |     |   |     |    |                                                                    |
|---------|-----|---|-----|----|--------------------------------------------------------------------|
| ModPrsL | VOL | 0 | 0.4 | %  | IOL=2.0mA                                                          |
|         | VOH |   |     | dB | ModPrsL can be implemented as a short-circuit to GND on the module |

## 10. High Speed Electrical Signal

| Parameter                                           | Min                         | Typical | Max  | Unit | Notes |
|-----------------------------------------------------|-----------------------------|---------|------|------|-------|
| Receiver electrical output characteristics at TP4   |                             |         |      |      |       |
| Signaling rate per lane                             |                             | 53.125  |      | GBd  |       |
| AC common-mode output voltage(RMS)                  |                             | -       | 17.5 | mV   |       |
| Differential peak-to-peak output voltage            |                             |         | 900  | mV   |       |
| Near-end ESMW (Eye symmetry mask width)             |                             | TBD     |      | UI   |       |
| Near-end Eye height, differential                   | 24                          |         |      | mV   |       |
| Near-end vertical eye closure                       |                             |         | 7.5  | dB   |       |
| Far-end ESMW (Eye symmetry mask width)              |                             | TBD     |      | UI   |       |
| Far-end Eye height, differential                    | 24                          |         |      | mV   |       |
| Far-end vertical eye closure                        |                             |         | 7.5  | dB   |       |
| Far-end pre-cursor ISI ratio                        |                             | TBD     |      | %    |       |
| Common mode to differential conversion return loss  | 802.3ck 120G-1              |         |      | dB   |       |
| Effective return loss                               | TBD                         |         |      | dB   |       |
| Differential termination mismatch                   |                             |         | 10   | %    |       |
| Transition time (min, 20% to 80%)                   |                             | TBD     |      | ps   |       |
| DC common mode voltage                              | -350                        |         | 2850 | mV   |       |
| Transmitter electrical input characteristics at TP1 |                             |         |      |      |       |
| Signaling rate, per lane                            |                             | 53.125  |      | GBd  |       |
| Differential pk-pk input voltage tolerance          | 900                         |         |      | mV   |       |
| Common-mode to differential return loss             | 802.3ck<br>Equation(120G-1) |         |      |      |       |
| Effective return loss                               | TBD                         |         |      |      |       |
| Differential termination mismatch                   |                             |         | 10   | %    |       |
| Module stressed input test                          | See 120G.3.4.1              |         |      |      |       |
| Single-ended voltage tolerance range                | -0.4                        |         | 3.3  | V    |       |
| DC common-mode voltage                              | -350                        |         | 2850 | mV   |       |

## 11. Receiver Thresholds for Loss of Signal (LOS)

| Parameter                | Min | Typical | Max  | Unit |
|--------------------------|-----|---------|------|------|
| RX_LOS_Assert Min/Max    | -15 |         |      | dBm  |
| RX_LOS_De-Assert Min/Max |     |         | -8.9 | dBm  |

|                   |  |     |  |    |
|-------------------|--|-----|--|----|
| RX_LOS_Hysteresis |  | 1.5 |  | dB |
|-------------------|--|-----|--|----|

## 12. Digital Diagnostic Monitoring Specifications

| Parameters                                 | Unit | Specification |
|--------------------------------------------|------|---------------|
| Temperature Monitor absolute error         | °C   | ± 3           |
| Supply Voltage Monitor absolute error      | %    | ± 5           |
| I <sub>bias</sub> Monitor absolute error   | %    | ± 10          |
| Received Power (Rx) Monitor absolute error | dB   | ± 3.0         |
| Transmit Power (Tx) Monitor absolute error | dB   | ± 3.0         |

## 13. Edge Connector and Pinout Description

The electrical pinout is shown in Figure 1 below.

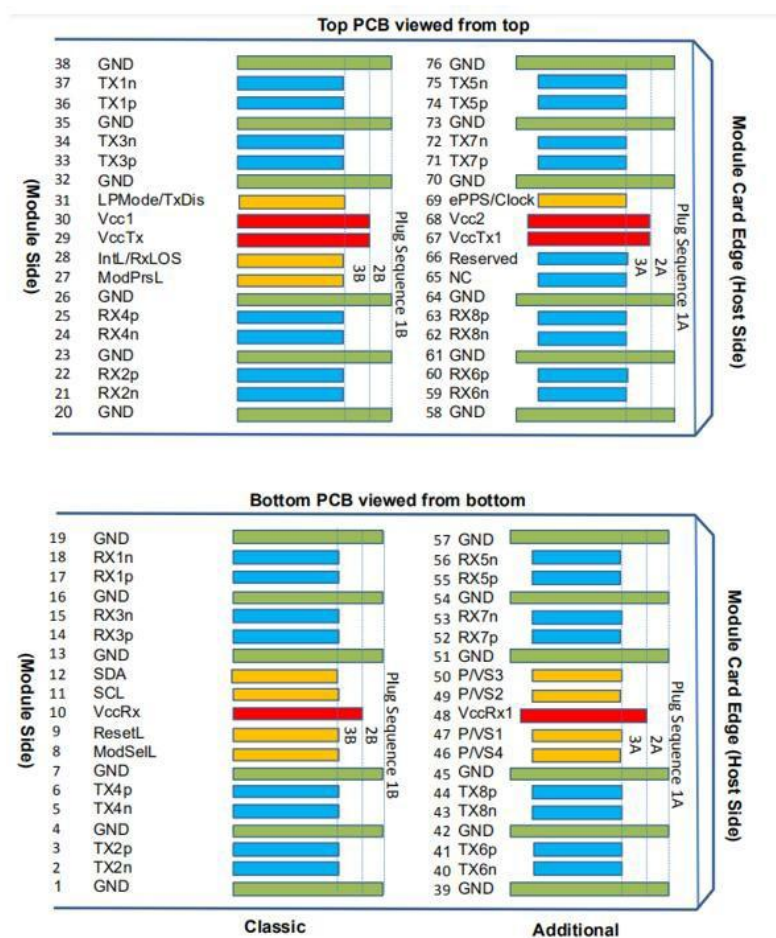


Figure 1. QSFP-DD 112 contact assignment

### Pad Function Definition

| Pad | Logic | Symbol | Description                     | Plug Sequence <sup>4</sup> | Notes |
|-----|-------|--------|---------------------------------|----------------------------|-------|
| 1   |       | GND    | Ground                          | 1B                         |       |
| 2   | CML-I | Tx2n   | Transmitter Inverted Data Input | 3B                         |       |

|    |            |                  |                                     |    |   |
|----|------------|------------------|-------------------------------------|----|---|
| 3  | CML-I      | Tx2p             | Transmitter Non-Inverted Data Input | 3B |   |
| 4  |            | GND              | Ground                              | 1B |   |
| 5  | CML-I      | Tx4n             | Transmitter Inverted Data Input     | 3B |   |
| 6  | CMI-I      | Tx4p             | Transmitter Non-Inverted Data Input | 3B |   |
| 7  |            | GND              | Ground                              | 1B |   |
| 8  | LVTTL-I    | ModSelL          | Module Select                       | 3B |   |
| 9  | LVTTL-I    | ResetI           | Module Reset                        | 3B |   |
| 10 |            | VccRx            | +3.3V Power Supply Receiver         | 2B | 2 |
| 11 | LVC MOS-VO | SCL              | TWI serial interface clock          | 3B |   |
| 12 | LVC MOS-VO | SDA              | TWI serial interface data           | 3B |   |
| 13 |            | GND              | Ground                              | 1B | 1 |
| 14 | CML-O      | Rx3p             | Receiver Non-Inverted Data Output   | 3B |   |
| 15 | CML-O      | Rx3n             | Receiver Inverted Data Output       | 3B |   |
| 16 |            | GND              | Ground                              | 1B | 1 |
| 17 | CML-O      | Rx1p             | Receiver Non-Inverted Data Output   | 3B |   |
| 18 | CML-O      | Rx1n             | Receiver Inverted Data Output       | 3B |   |
| 19 |            | GND              | Ground                              | 1B | 1 |
| 20 |            | GND              | Ground                              | 1B |   |
| 21 | CML-O      | Rx2ni            | Receiver Inverted Data Output       | 3B |   |
| 22 | CML-O      | Rx2p             | Receiver Non-Inverted Data Output   | 3B |   |
| 23 |            | GND              | Ground                              | 1B | 1 |
| 24 | CML-O      | Rx4n             | Receiver Inverted Data Output       | 3B |   |
| 25 | CML-O      | Rx4p             | Receiver Non-Inverted Data Output   | 3B |   |
| 26 |            | GND              | Ground                              | 1B | 1 |
| 27 | LVTTL-O    | ModPrsL          | Module Present                      | 3B |   |
| 28 | LVTTL-O    | IntL/RxLOS       | Interrupt/optional RxLOS            | 3B | 2 |
| 29 |            | VccTx            | +3.3V Power supply transmitter      | 2B |   |
| 30 |            | Vcc1             | +3.3V Power supply                  | 2B | 2 |
| 31 | LVTTL-I    | LPMode/<br>TxDis | Low Power mode/optional TX Disable  | 3B |   |
| 32 |            | GND              | Ground                              | 1B | 1 |
| 33 | CML-I      | Tx3p             | Transmitter Non-Inverted Data Input | 3B |   |
| 34 | CML-I      | Tx3n             | Transmitter Inverted Data Input     | 3B |   |

|    |                |        |                                       |    |   |
|----|----------------|--------|---------------------------------------|----|---|
| 35 |                | GND    | Ground                                | 1B | 1 |
| 36 | CML-I          | Tx1p   | Transmitter Non-Inverted Data Input   | 3B |   |
| 37 | CML-I          | Tx1n   | Transmitter Inverted Data Input       | 3B |   |
| 38 |                | GND    | Ground                                | 1B | 1 |
| 39 |                | GND    | Ground                                | 1A | 1 |
| 40 | CML-I          | Tx6n   | Transmitter Inverted Data Input       | 3A |   |
| 41 | CML-i          | Tx6p   | Transmitter Non-Inverted Data Input   | 3A |   |
| 42 |                | GND    | Ground                                | 1A |   |
| 43 | CML-I          | Tx8n   | Transmitter Inverted Data Input       | 3A |   |
| 44 | CML-I          | Tx8p   | Transmitter Non-Inverted Data Input   | 3A |   |
| 45 |                | GND    | Ground                                | 1A |   |
| 46 | LVC MOS /CML-I | P/VS4  | Programmable/Module Vendor Specific 4 | 3A | 5 |
| 47 | LVC MOS /CML-I | P/VS1  | Programmable Module Vendor Specific 1 | 3A | 5 |
| 43 |                | VccRx1 | 3.3V Power Supply                     | 2A | 2 |
| 49 | LVC MOS /CML-O | P/VS2  | Programmable/Module Vendor Specific 2 | 3A | 5 |
| 50 | LVC MOS /CML-O | P/VS3  | Programmable Module Vendor Specific 3 | 3A | 5 |
| 51 |                | GND    | Ground                                | 1A | 1 |
| 52 | CML-O          | Rx7P   | Receiver Non-Inverted Data Output     | 3A |   |
| 53 | CML-O          | Rx7n   | Receiver Inverted Data Output         | 3A |   |
| 54 |                | GND    | Ground                                | 1A | 1 |
| 55 | CML-O          | Rx5p   | Receiver Non-Inverted Data Output     | 3A |   |
| 56 | CML-O          | Rx5n   | Receiver Inverted Data Output         | 3A |   |
| 57 |                | GND    | Ground                                | 1A | 1 |
| 53 |                | GND    | Ground                                | 1A | 1 |
| 59 | CML-O          | Rx6n   | Receiver Inverted Data Output         | 3A |   |
| 60 | CML-O          | Rx6p   | Receiver Non-Inverted Data Output     | 3A |   |
| 61 |                | GND    | Ground                                | 1A | 1 |
| 62 | CML-O          | Rx8n   | Receiver Inverted Data Output         | 3A |   |
| 63 | CML-O          | Rx8p   | Receiver Non-Inverted Data Output     | 3A |   |

|    |           |            |                                         |    |   |
|----|-----------|------------|-----------------------------------------|----|---|
| 64 |           | GND        | Ground                                  | 1A | 1 |
| 65 |           | NC         | No Connect                              | 3A | 3 |
| 66 |           | Reserved   | For future use                          | 3A | 3 |
| 67 |           | VccTx1     | 3.3V Power Supply                       | 2A | 2 |
| 63 |           | Vcc2       | 33V Power Supply                        | 2A |   |
| 69 | LVC MOS-I | ePPS/Clock | 1PPS PTP clock or reference clock input | 3A | 6 |
| 70 |           | GND        | Ground                                  | 1A | 1 |
| 71 | CML-I     | Tx7p       | Transmitter Non-Inverted Data Input     | 3A |   |
| 72 | CML-I     | TX7n       | Transmitter Inverted Data Input         | 3A |   |
| 73 |           | GND        | Ground                                  | 1A | 1 |
| 74 | CML-I     | Tx5p       | Transmitter Non-Inverted Data Input     | 3A |   |
| 75 | CML-I     | Tx5n       | Transmitter Inverted Data Input         | 3A |   |
| 76 |           | GND        | Ground                                  | 1A | 1 |

#### Notes:

Note 1: QSFP-DD uses common ground(GND)for all signals and supply (power).All are common within the QSFP-DD module and all module voltages are reference to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady slate current of 500 mA.

Note 2: VocRx,VocRx1,Vec1,Vec2,VocTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card edge Connector are listed in Table 13.For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA

Note 3: Reserved and no Connect pads recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect)shall be left unconnected within the module.

Note 4: Plug Sequence specifies the mating sequence cf the host connector and module. The sequence s 1A,2A,3A 1B,2B,3B.(see Figure 2 for pad locations)Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 13 will then occur simultaneously, followed by 2A and 2B,followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10kΩ.

Note 6: ePPS/Clock if not used recommended to be terminated with 50 Q to ground on the host

## 14. Module Block Diagram

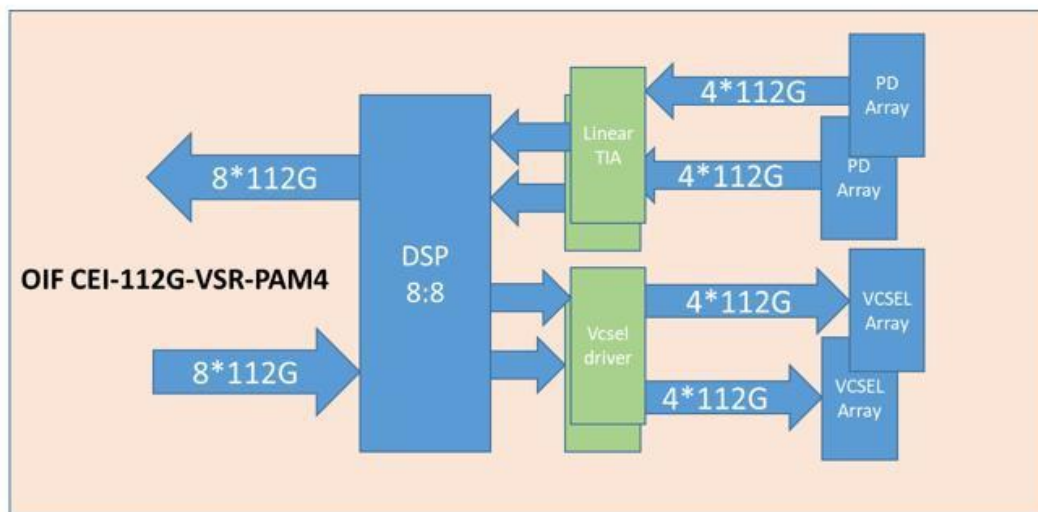


Figure 2. Module Block Diagram

## 15. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## 16. Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No.50, dated (June 24, 2007).

Caution: use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## 17. Optical Interface

The eight transmit and eight receive optical lanes of the module occupy the positions depicted in Figure 3 when looking into the MPO16 receptacle with the connector keyway feature on top.

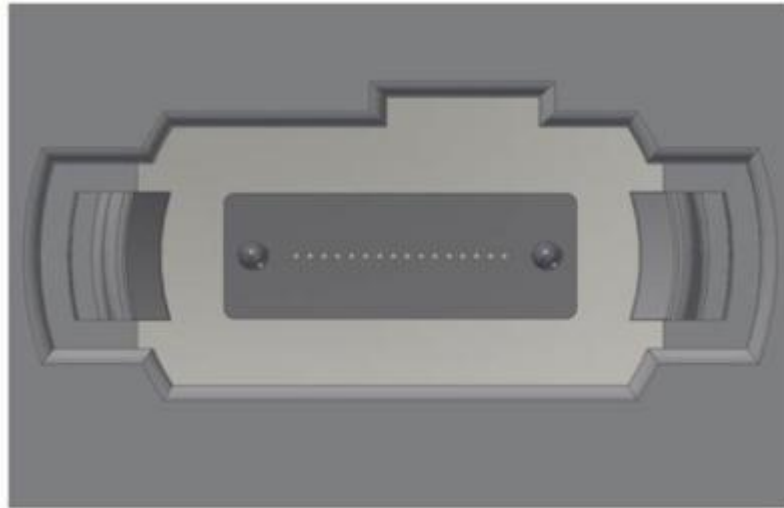


Figure 3. Optical lane assignments

## 18. Mechanical Dimensions

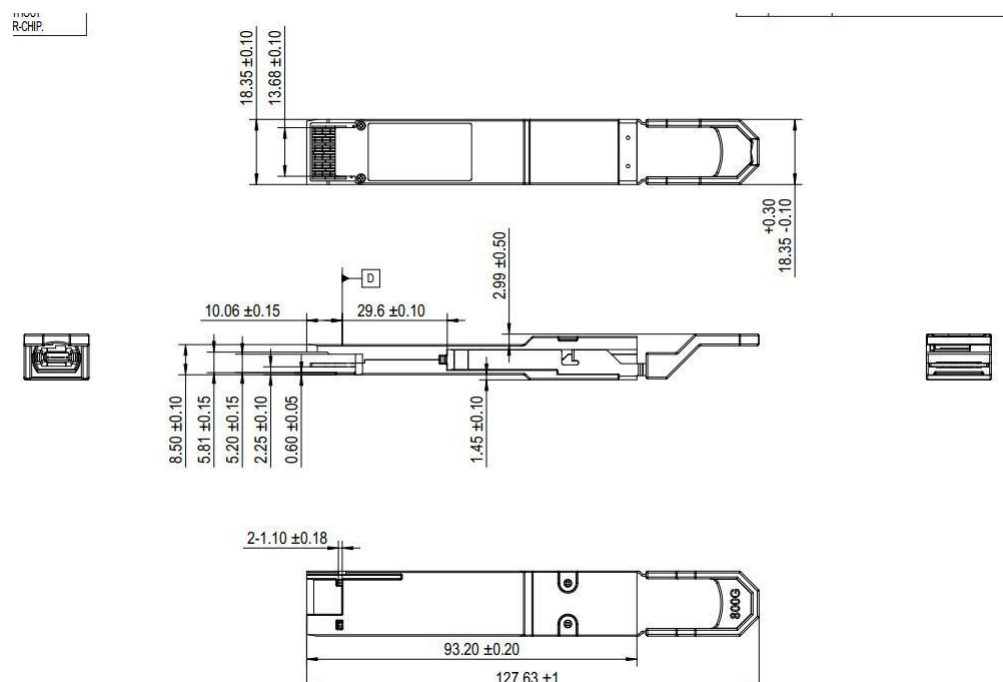


Figure 4. Mechanical outline.

## 19. Ordering information

| Product Description                  | Part Number  |
|--------------------------------------|--------------|
| 800G QSFP-DD SR8 Optical Transceiver | QDD-800G-SR8 |